

ABSTRACT OF THE DISCLOSURE

A phase difference detector adapted to generating a signal indicative of a phase difference between a first signal and a second signal, comprising: a first bistable element clocked by the first signal and having a first output signal, and a second bistable element clocked by the second signal and having a second output signal; means for determining the variation of the signal indicative of the phase difference, responsive to the first and second output signals, and a reset circuit having a first and a second inputs respectively connected to the first and second output signals and adapted to determine the resetting of the first and second bistable elements in response to the attainment of a respective prescribed state by the first and the second output signals. The first and second inputs of the reset circuit are substantially symmetrical to each other from the point of view of an input impedance associated to each of them.

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